ABSTRACT OF THE DISCLOSURE

An amplifier circuit having an output delay that is selectively changed in accordance with a common mode voltage level. A replica delay circuit adapted for use within an internal clock generator include such an amplifier circuit. The amplifier circuit includes a first amplifier generating internal signal in response to input signals changes a common mode voltage level of the internal signals in response to control signals. The amplifier also includes a second amplifier comparing voltage levels of the internal signals, generating an output signal in accordance with a comparison result, and changing a duty cycle of the output signal when the common mode voltage level of the internal signals is changed.